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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,289	02/15/2002	Sylvie Lesmanne	T2147-907715	9018

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EXAMINER	
HO, THANG H	

ART UNIT	PAPER NUMBER
2188	3

DATE MAILED: 11/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,289	LESMANNE ET AL.	
	Examiner	Art Unit	
	Thang H Ho	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed on 02/15/2002.

Information Disclosure Statement

2. The information disclosure statement (IDS) filed on 07/11/2002 has been received and considered. Please see attached PTO-1449.

3. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Drawings

4. The formal drawings have been reviewed by the United Sates Patent and Trademark Office of Draftperson's Patent Drawings Review.

5. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

6. Claims 1-12 are presented for examination.

7. On page 8, paragraph numbered 30, the recitation of "retrys" should be changed to read --retries--.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ekanadham et al. (USPN: 6,085,295), hereinafter Ekanadham.

As per claim 1, Ekanadham discloses in FIG. 1 a coherence controller connected to multiprocessors (PN) within a local module (NODE N), the multiprocessor (PN) including a local main memory (MN) and a plurality of processors (PN) each equipped with a cache memory (column 2, lines 25-26 *"...remote line is brought into the cache of a processor..."*), the coherence controller comprising:

- a cache filter directory (embedded within adapter "A") including a first filter directory for guaranteeing coherence between the local main memory (MN) and the cache memory in each of the processors of the local module (NODE N) [(Ekanadham, FIG. 4, column 1, lines 35-37 *"The adapter maintains a directory of all nodes..."* and column 3, lines 57-64 *"FIG. 4 illustrates... It comprises a set of node lists **41** and local... cached by the local processors."*)];

- a complementary filter directory (embedded within adapter "A") for tracking locations of lines or blocks of the local main memory copied from the local module into at least one external module and for guaranteeing coherence between the local main memory and the cache in each of the processors of the local module and said at least one external module [(Ekanadham, FIG. 4, column 1, lines 35-37 *"The adapter maintains a directory of all nodes..."* and column 3, lines 57-64 *"FIG. 4 illustrates... It comprises a set of node lists **41** and local... cached by the local processors."*)]; and an
- external port connected to said at least one external module [(Ekanadham, FIG. 1, element A)].

As per claim 2, Ekanadham discloses in FIG. 4 the cache filter directory includes: an "n"-bit presence vector (42) where n is a number of multiprocessors in the local module, an "n-1"-bit extension of the presence vector (41), where n-1 is a total number of external modules connected to the external port, and an Exclusive status bit (43) [(Ekanadham, FIG. 4, column 3, lines 59-64 *"It comprises... node lists **41**... processor lists **42**... 2-bit line state directory **43**..."*)].

As per claim 3, Ekanadham discloses in FIG. 1 the external port (A) is connected directly or indirectly to the external modules (NODE N) via an external two-point link (NETWORK).

As per claim 4, Ekanadham discloses in FIG. 1 a coherence controller further comprising: "n" control units connected to the "n" multiprocessors in the local module (NODE N), a control unit XPU connected to the external port (embedded within adapter A), and a common control unit containing the cache filter directory (FIG. 4) [(Ekanadham, column 1, lines 59-62 *"Each processor communicates... via the switch"* and column 2, lines 52-55 *""When a memory command is issued from... a node to a memory of another node, the command is directed to an adapter...*). Note that all controlling units within claim 4 are embedded within adapter "A"].

As per claim 5, Ekanadham discloses that the control unit XPU and the "n" control units are compatible with one another and use similar protocols [(Ekanadham, column 3, lines 39-41 *"...the adapter uses the local SMP coherence protocol..."*)].

As per claim 6, Ekanadham discloses in FIG. 1 a multiprocessor module (e.g. NODE 1) connected to a coherence controller [(NODE 1 is connected to adapter "A" via a switch device "SWITCH")].

As per claim 7, Ekanadham discloses in FIG. 1 a multiprocessor system with a multimodule architecture, comprising: at least two multiprocessor modules (NODE 1 – NODE 3) connected to one another through external ports (A) of coherence controllers located within said at least two multiprocessor modules.

As per claim 8, Ekanadham discloses in FIG. 1 the external ports (A) are connected to one another through a switching device or router (NETWORK).

As per claim 9, Ekanadham discloses in FIG. 1 a switching device or a router (A) which manages and/or filters data and/or requests in transit between two multiprocessor modules (e.g. NODE 1 and NODE 2) [(Ekanadham, Column 49-55 *"The adapter connects to the switch... behaves as proxy processor..."*)].

As per claim 10, Ekanadham discloses in FIG. 1 a multimodule architecture, comprising:

- a plurality of multiprocessor modules (NODE N) wherein the multiprocessor modules include:
  - a plurality of multiprocessors (PN) each equipped with at least one cache memory and at least one local main memory, and a local coherence controller (A) connected to the multiprocessors and including a local cache filter directory (FIG.1 element A and FIG. 4), for guaranteeing local coherence between the local main memory (MN) and the cache memories in each of the multiprocessors (column 2, lines 25-26 *"...remote line is brought into the cache of a processor..."*), said local coherence controller connected to at least a second one of said multiprocessor modules (FIG.1, NODEN), wherein the coherence controller further includes:

- a complementary cache filter directory for tracking a location of memory lines or blocks copied from said first multiprocessor module (NODE 1) to the second one (NODE 2) of the multiprocessor modules and for guaranteeing coherence between the local main memory (MN) and the cache memories in each of the multiprocessors in the first module (NODE 1) and the second one (NODE 2) of the multiprocessor modules (NODE N) [(Ekanadham, FIG. 4, column 1, lines 35-37 *"The adapter maintains a directory of all nodes..."* and column 3, lines 57-64 *"FIG. 4 illustrates... It comprises a set of node lists **41** and local... cached by the local processors."*)].

As per claim 11, Ekanadham discloses a multimodule architecture, wherein the coherence controller includes: an "n"-bit presence vector (42) which indicates presence or absence of a copy of a memory block or line in the cache memories of the multiprocessors, an "n-1"-bit extension of the presence vector (41) which indicates presence or absence of a copy of a memory block or line in cache memories of multiprocessors in the second one of said multiprocessor modules, and an Exclusive status bit (43) [(Ekanadham, FIG. 4, column 3, lines 59-64 *"It comprises... node lists **41**... processor lists **42**... 2-bit line state directory **43**..."*)].

As per claim 12, Ekanadham discloses in FIG. 1 a multimodule architecture further comprising: switching device or router (A) which connects the first

multiprocessor module (NODE 1) with the second one (NODE 2) of the multiprocessor modules (NODE N), the switching device or router (A) including a unit which manages and/or filters data and/or requests in transit between the first multiprocessor module and the second one of said multiprocessor modules [(Ekanadham, Column 49-55 *"The adapter connects to the switch... behaves as proxy processor..."*)].

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form PTO-892.

11. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to (703) 872-9306

Hand–delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. Sixth Floor (Receptionist).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 703-305-1888. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-6606 for regular communications and 703-308-9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Thang Ho
Art Unit 2188
October 31, 2003

Mano Padmanabhan
10/31/03

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
TC 2100